Cadence VLSI and Embedded System Design Centre

Center of Excellence for Electronics and Telecommunication
at
SGIARC-TBI Foundation, Shegaon

Cadence VLSI and Embedded System Design Centre is Center of Excellence for Electronics and Telecommunication established in 2006 at SGIARC-TBI Foundation, Shegaon is equipped with equipped with world-renowned Cadence EDA tools, is a pivotal resource for fostering excellence in analog, digital, and mixed-signal IC design. The Cadence VLSI and Embedded Design Lab is a cornerstone of advanced engineering education, providing students with the tools and knowledge necessary to excel in the semiconductor industry. The lab's capabilities and the hands-on experience it offers are invaluable for preparing the next generation of VLSI designers. This lab not only contributes to individual student success but also to the broader goal of technological self-reliance and innovation in India. A detail report on this lab is outlined below:

1. Introduction

The Cadence VLSI and Embedded Design Lab is equipped with world-renowned Cadence VLSI EDA (Electronic Design Automation) tools. These tools are integral for Application-Specific Integrated Circuit (ASIC) design, encompassing analog, digital, and mixed-signal IC design. The lab is a significant asset for engineering education, providing students with hands-on experience in state-of-the-art technologies used in the semiconductor industry.

2. Importance of Cadence EDA Tools

Cadence EDA tools are indispensable for the modern VLSI design ecosystem. They provide a comprehensive suite of software applications that automate the complex process of designing integrated circuits. Key benefits include:

2.1 Industry Standard Tools: Cadence tools are widely recognized and used in the semiconductor industry for designing and verifying integrated circuits. Familiarity with these tools prepares students for careers in top tech companies.

2.2 Comprehensive Design Solutions: The tools support the entire design flow, from initial design specification to final verification and testing, ensuring students understand the complete lifecycle of IC design.

2.3 Advanced Capabilities: The tools include advanced features for simulation, synthesis, layout, and verification, providing students with the ability to work on complex design projects.

2.4 Accelerated Time-to-Market: By streamlining the design flow, Cadence tools contribute to faster product development and quicker market entry.

2.5 Complex Design Handling: The tools can handle the increasing complexity of modern ICs, enabling the design of sophisticated systems-on-chip (SoCs).

3. Uses of the Facilities

3.1 Analog IC Design: Tools such as Cadence Virtuoso enable students to design and simulate analog circuits, including amplifiers, oscillators, and filters.

3.2 Digital IC Design: Tools like Cadence Genus and Innovus facilitate the design and implementation of digital circuits, from RTL synthesis to place and route.

3.3 Mixed-Signal Design: The lab supports mixed-signal design projects, integrating both analog and digital components, which are critical for modern electronics such as ADCs and DACs.

3.4 Verification and Testing: Cadence tools provide robust verification environments, including functional verification with Cadence Xcelium and formal verification with Cadence JasperGold.

4. Benefits for Students

4.1 Hands-On Experience: Students gain practical experience with tools and methodologies used in the industry, bridging the gap between theoretical knowledge and real-world applications.

4.2 Skill Development: Working with Cadence tools enhances students' skills in VLSI design, simulation, and verification, making them highly competitive in the job market.

4.3 Research Opportunities: The lab enables students to undertake advanced research projects in VLSI design, contributing to academic and industry advancements.

4.4 Collaboration: The lab fosters collaboration between students, faculty, and industry experts, promoting knowledge exchange and innovation.

5. Future Importance

5.1 Technological Advancements: As technology continues to evolve, proficiency in VLSI design tools remains crucial for developing cutting-edge electronic devices.

5.2 Industry Demand: The demand for skilled VLSI designers is expected to grow, driven by the increasing complexity of electronic systems and the proliferation of IoT, AI, and 5G technologies.

5.3 Innovation: Future innovations in electronics heavily rely on advanced IC design. Training students with these tools ensures a continuous pipeline of skilled professionals contributing to technological advancements.

6. Government of India Initiatives

6.1 Make in India: The initiative promotes domestic manufacturing and design, encouraging the development of indigenous technologies and reducing dependency on imports.

6.2 Digital India: Aims to transform India into a digitally empowered society. Skilled VLSI designers are essential for developing the infrastructure required for this transformation.

6.3 Startup India: Supports the creation of new businesses and innovations in the technology sector, including semiconductor startups focusing on IC design and fabrication.

6.4 Skill India: Focuses on skill development, including training in advanced technologies like VLSI design, ensuring the availability of a skilled workforce to support the country's technological ambitions.

7. Overall Outcome of this lab

SN	Heads	Numbers	Last Five Years
1	No of Phds	04	01
2	PG/UG Projects	10	03
3	No of Publications	27	16
4	No of Training Programs	05	02
5	No of R&D Proposals Submitted	04	02
6	No of collaborations	04	02
7	Awards/Recognition/Achievement	04	03

7.1 List of PhD Thesis

Sn	Title	Submitted by	Guided by	Submitted to	Remark
1	Design and Performance Analysis of Digital Radio Frequency Memory (DRFM) System For Mobile Communication	Santosh B. Patil	Dr. R. D. Kanphade	S.G.B., Amravati University, Amravati 2016	Degree awarded
2	Design, Development of Reconfigurable Mixed Signal and Adoptive Digital Filters	Mahesh B. Dembrani	Dr. K. B. Khanchandani	S.G.B., Amravati University, Amravati 2016	Degree awarded
3	Design, Development and Performance Analysis CMOS Phase Locked Loop Synthesizer for Wireless Applications	Priti N. Metange	Dr. K. B. Khanchandani	S.G.B., Amravati University, Amravati 2017	Degree awarded
4	Optimized of Polar Code Deceoder for 5G Wireless Applications and Its performance Evaluation	Swapnil B. Badar	Dr. K. B. Khanchandani	S.G.B., Amravati University, Amravati 2024	Thesis Submitted

7.2 Project Carried Out

Sn	Title	Name of Students	Guided By	Year
1	Design of Operational Trnsconductance Amplifier	Mr. Amit Khade Mr. Sanjeev Ranjan Ms. Pritee Gawande	Dr. Rajendra D. Kanphade, Dr. Maryam Shojaei Baghini and Dr. Santosh B. Patil	2006-2007
2	Design and Simulation of Cascode LNA working on 2.4Ghz	Mr. Chetan More Ms. Jaishree Suryawanshi Ms. Rashmi Jain	Dr. Santosh B. Patil	2012-2013
3	Design and Simulation of Programmable Pulse Generator	Mr. Vaibhav Waghode Mr. Satish Tapre Mr. Rushikesh Mr. Adekar Mr. Pravin S. Pawar Mr. Sachin Belokar	Dr. Santosh B. Patil	2012-2013

4	Design and Analysis of Cascade Power Amplifier on 2.4Ghz Frequency Applications	Aditya Pathak Akesh Rathod Anagh Deshpande Pradip H. Dhakre	Prof. V. V. Ratniparkhi	2012-2013
5	Register Based SPI Interface	Rushi Vyas Priya Agnani Marshal Anthony	Prof. V. N. Bhonge	2012-2013
6	Design of Asynchronous First- in-first-out (FIFO)	Jaysen Ambade Pradnya Chikate Mayur Suryawanshi Meenal Bhirad Akash Chillure	Prof. V. K. Bhangdiya	2012-2013
7	Design and Implementation of CMOS Doherty Power Amplifier for 2.4Ghz Frequency Applications	Mr. Siddhant Rahud Mr. Nikhil Nakade Mr. Nishikant Dhabekar Mr. Mahesh Pithe Mr. Prashant Chambhare	Dr. Santosh B. Patil	2013-2014
8	Transceiver IF IC Development For 5G mm Wave Radio	Ms. Apeksha Mali Ms. Chaitalee Hedau Mr. Darshan patil Mr. Kartik Agrawal Mr. Nitin Katole Ms. Priyanka Wakode Ms. Savita Nikhade	Dr. Santosh B. Patil	2018-2019
9	Real Time Implementation of BPSK Modulation and Demodulation Scheme on Spartan- 3 FPGA using Mixed HDL Simulink Platform	Mr. Sachin R. Ambadkar	Dr. Santosh B. Patil	2020-2021
10	Current Controlled Current Differencing Transconductance Amplifier for Analog Signal Processing	Mr. Vishnu Mathariya Mr. Abhijeet Jawanjalkar Ms. Trupti Gawande Ms. Srushti Thorat	Prof. S. P. Badar	20121-2022

7.3 List of Publications

Sn	Paper Details	Year
1	D. Kanphade, S. B. Patil, A. M. Patokar and D.D. Nawgaje, "FPGA Prototype Of 14 Bit, 20msamples/S, 85 Mw Successive Approximation ADC Suitable For RF Applications", ICWET '11 Proceedings of the International Conference & Workshop on Emerging Trends in Technology, Pp 832-836 Mumbai, Maharashtra, India — February 25 - 26, 2011 ACM New York, NY, USA ©2011. (Published in ACM Digital Library)	2011
2	Dr. R. D. Kanphade, S. B. Patil and Rohan Musale, "Design	2013

	and Implementation of Memory Interface Controller with SRAM Memory," International Journal of Engineering Research and Development e, Volume 6, Issue 1, PP. 15-20, February 2013,ISSN: 2278-067X, p-ISSN: 2278-800X.	
3	Dr. R. D. Kanphade, S. B. Patil and Rohan Musale, "Memory Interface Controller using Xilinx's Spartan family FPGA with SRAM Memory", IEEE sponsored, International Conference on Control, Computing, Communication and Materials (ICCCCM), August 03-04, 2013.	2013
4	S. B. Patil and R. D. Kanphade, "Design and analysis of a 2.4 GHz fully integrated 1.8V power amplifier in TSMC 180nm CMOS RF process for wireless communication," Proceedings of the VLSI Systems, Architecture, Technology and Applications IEEE International Conference (VLSI-SATA-2015), pp. 1 –5, 8 10 Jan. 2015, ISBN: 978-1-4799-7925-7 (Published in IEEE Xplore).	2015
5	Rajendra D. Kanphade and Santosh B. Patil, "Design Of A Transmit-Receive (T/R) Switch In TSMC 180nm RF CMOS Process For 2.4GHz Transceiver," Proceedings of the IEEE 2nd International Conference on Signal Processing and Integrated Networks (SPIN- 2015), pp. 881 – 886, 19-20 Feb. 2015, ISBN: 978-1-4799-5990-7 (Published in IEEE Xplore).	2015
6	Santosh B. Patil and Rajendra D. Kanphade, "Differential Input Differential Output Low Power High Gain LNA For 2.4 GHz Applications Using TSMC 180nm CMOS RF Process", Proceedings of the IEEE International Conference on Computing Communication Control and Automation (ICCUBEA-2015), pp. 911 – 916, 26-27 Feb. 2015. (Published in IEEE Xplore)	2015
7	Santosh B. Patil and Rajendra D. Kanphade ," A 2.4 GHz Double Balanced Differential Input Single Output Low Power Transmitting Mixer In TSMC 180nm CMOS RF Process", Proceedings of the IEEE 2nd International Conference on Electronics and Communication Systems (ICECS- 2015), pp. 1181 – 1186, 26-27 Feb. 2015, ISBN: 978-1-4799-7224-1 (Published in IEEE Xplore)	2015
8	Rajendra D. Kanphade and Santosh B. Patil , "A 2.4 GHz Double Balanced Differential Input Differential Output Low Power High Gain Gilbert Cell Down Conversion Mixer In TSMC 180nm CMOS RF Process", Proceedings of the IEEE 2nd International Conference on Electronics and Communication Systems (ICECS 2015), pp. 1187 - 1193, 26-27 Feb. 2015, ISBN: 978-1-4799-7224-1 (Published in IEEE Xplore)	2015
9	Santosh B. Patil , Rajendra D. Kanphade and Vivek V. Ratnaparkhi, "Design And Performance Analysis Of Inset Feed Microstrip Square Patch Antenna For 2.4GHz Wireless Applications", Proceedings of the IEEE 2nd International Conference on Electronics and Communication Systems (ICECS-2015), pp. 1194 - 1200, 26-27 Feb. 2015, ISBN: 978-1-4799-7224-1 (Published in IEEE Xplore)	2015

10	S. P. Badar and K. Khanchandani, "Implementation of Combinational Logic for Polar Decoder", 2021 2nd International Conference on Range Technology (ICORT), Chandipur, Balasore, India, 2021, pp. 1-6. (Received Best Paper Award)	2021
11	S. P. Badar and K. Khanchandani, "Successive Cancellation Polar Decoder Implementation using Processing Elements", 2022 IEEE Region 10 Symposium (TENSYMP), Mumbai, India, 2022, pp. 1-6.	2022
12	S. P. Badar and K. Khanchandani, "Analyzing Polar Decoding Approaches: A Comparative Study", Journal of VLSI Design and Signal Processing, 9(3), 2023, pp. 37-47.	2023
13	S. P. Badar, K. B. Khanchandani, P. R. Wankhede, "A Brief Study of Successive Cancellation Polar Decoder: Design and Performance Analysis", SSGM Journal of Science and Engineering, Vol. 1 No. 1 2023, pp.-146-150.	2023
14	S. P. Badar, K. Khanchandani and P. Wankhede, "Fast Polar Decoder Implementation using Special Nodes", 2023 2nd International Conference on Paradigm Shifts in Communications Embedded Systems, Machine Learning and Signal Processing (PCEMS), Nagpur, India, 2023, pp. 1-6.	2023
15	S. P. Badar and K. Khanchandani, "High Performance Polar Code Decoder for 5G Wireless Applications: Real Time Design and Development", at Aawishkar, University level Innovation Symposium, (Poster Presentation), 2023.	2023
16	S. P. Badar, K. B. Khanchandani, P. R. Wankhede "Efficient Implementation of Polar Decoder: Design and Performance Analysis", Lecture Notes on Network System, Springer Publication (Publish in July 2024).	2024

7.4 Training Programs Conducted

Sn.	Title	Resource Person	Duration	No of Students	Year
1	Basics of CMOS Design using Cadence	Prof. S. P. Badar	3 Days	40	2023
2	Hands on VLSI Circuit Design Using Cadence	Prof. S. P. Badar	2 Days	42	2019
3	Essentials of Xilinx EDA Tool & FPGA Design	Prof. S. B. Patil	01 Month	14	2009
4	Certificate Course in VLSI Design	Prof. S. B. Patil	01 Month	15	2008
5	One Week National Workshop on VLSI Design Using Cadence Tools	Prof. R. D. Kanphade Prof. S. B. Patil	01 Week	30	2007

7.5 List of Research Proposal

Sn	Title	Principal Investigator	External Agency	Funding Agency	Amount and Year	Remark
1	ASIC Development of PLL Synthesizer for Multichannel FR1 Bands of 5G Technology	Dr. Santosh Balkrishna Patil, Principal Investigator, Dr. Ram S. Dhekekar, Co-Principal Investigator	Symbiosis Institute of Technology, Symbiosis International (Deemed University), Lavale Campus, Tal. Mulshi, Pune	CHIP TO STARTUP (C2S) PROPOSAL MeitY, Gov. of India	Rs 1.00 Cr 2023	Presented but proposal not granted for the funding Synopsis EDA tool Sanctioned.
2	Fully Integrated Compact Multimode Multiband Transceiver Front-end Model (FEM) For 3G/4G Applications	Dr. Santosh Balkrishna Patil & Dr. S. M. Moghe	S M Wireless Technology Pvt. Ltd., Nagpur	Science and Engineering Research Baord (SERB), New Delhi	Rs 2.16 Cr 2022	Presented but not recommended for financial grant.
3	Development Of Millimeter Wave (60GHz) Transceivers For High Data Rate (2 Gbps Or Higher) Communication System	Dr. Santosh Balkrishna Patil & Dr. S. M. Moghe	S M Wireless Technology Pvt. Ltd., Nagpur	DST, New Delhi (Technology System Development Program	Rs 2.00 Cr 2012	Presented but proposal not granted for the funding
4	A Low Power ZigBee Transceiver (915Mhz) for Home Area Network	Dr. Santosh Balkrishna Patil	NA	SGIARC, Shegaon And Student Contribution	Rs.10.00 Lakh 2014	Presented but not recommended for financial grant.

7.6 Collaborations

Sn	Title	Agency	Year
1	ASIC Development of PLL Synthesizer for Multichannel FR1 Bands of 5G Technology	Symbiosis Institute of Technology, Symbiosis International (Deemed University), Lavale Campus, Tal. Mulshi, Pune	2023
2	Fully Integrated Compact Multimode Multiband Transceiver Front-end Model (FEM) For 3G/4G Applications	S M Wireless Technology Pvt. Ltd., Nagpur	2022
3	Development Of Millimeter Wave (60GHz) Transceivers For High Data	S M Wireless Technology Pvt. Ltd., Nagpur	2010

	Rate (2 Gbps Or Higher) Communication System		
4	Design kits (Cadence and Synopsis) HCMOS9GP- ST Microelectronics 130nm	CMP Fab Lab, Grenoble, France	2015

7.7 Awards/Recognition/Achievement

Sn.	Title	Name of Person	Year
1	Project- Design of Operational Trnsconductance Amplifier Winner of first ever national level 'Cadence India Design Contest'. Won cash prize of Rs. 1.5 lack and reorganization at national level project competition organized by Cadence Design Systems (I) Pvt. Ltd., Bangalore, INDIA and CDNLive! India- part of Cadence's global series of technical conferences in 2006 https://www.business- standard.com/article/companies/cadence-announces- design-contest-winners-106101801011_1.html	Dr. Rajendra D. Kanphade Dr. Santosh B. Patil and Team	2006
2	Project- Design and Development of Analog Circuits Using Unconventional CMOS Techniques for Biomedical Applications Runner-up of Cadence Design Contest India 2018	Dr. K. B. Khanchandani , Prof. S. P. Badar and Team	2018
3	Successfully completed the " Training in Advanced Capabilities in Electronics Design & Manufacturing (TRIAC-EDM)" course during 13th - 17th Feb 2023 at YTL- IRI, National Taiwan University, Taipei, Taiwan . The training program was sponsored jointly by Industrial Development Bureau (Ministry of Economic Affairs), Ministry of Electronics & IT, Govt. of India, and implemented by Institute of Information Industry (III), National Institute of Electronics & Information Technology (NIELIT) and YEN-TJING LING Industrial Research Institute of National Taiwan University.	Dr. Santosh B. Patil	2023
4	Received Best Project award in the track "Analog IC Design" at Indian Institute of Information Technology (IIIT), Allahabad during their internship from 24 June to 21 July 2024	Mr. Soham Bhole Mrs. Janhvi Kokwar	2024